IN THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

Claim 1-27 (canceled).

28 (previously presented). A method of determining whether a programmable element in an integrated circuit has been programmed, comprising the acts of:

producing a first voltage at a first node based on a resistance of the programmable element;

producing a second voltage at a second node based on a known resistance; and

comparing the first and second voltages and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

29 (previously presented). The method of claim 28, comprising the acts of:

equilibrating the voltages at the first and second nodes; and

performing the act of comparing the first and second voltages after sufficient time has elapsed to allow the first and second voltages to change, respectively, based on the known resistance and the resistance of the programmable element.

30 (previously presented). The method of claim 29, wherein the voltages at the first and second nodes are equilibrated at the same approximate voltage between V_{CC} and zero volts.

31 (previously presented). A method of determining whether a programmable element in an integrated circuit has been programmed, the method comprising the acts of:

providing a first node at which a first voltage is produced based on a resistance of the programmable element;

providing a second node at which a second voltage is produced based on a known resistance;

equilibrating the voltages at the first and second nodes; and

comparing the voltages at the first and second nodes and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

32 (previously presented). An apparatus for determining whether a programmable element in an integrated circuit has been programmed, the apparatus comprising:

a programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element;

a reference generator adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparison circuit adapted to compare the voltage on the first node to the reference voltage on the second node and produce an output signal having a binary value indicative of whether the programmable element has been programmed.

33 (previously presented). The apparatus of claim 32, comprising an equilibrating circuit adapted to equilibrate the voltages at the first and second nodes.

34 (previously presented). The apparatus of claim 32, wherein the programmable element comprises an antifuse element.

35 (previously presented). The apparatus of claim 32, wherein the programmable element comprises an ovonic element.

36 (previously presented). In an integrated circuit, an apparatus comprising:

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all the plurality of programmable circuits being joined in a common connection;

selection circuitry adapted to select one of the plurality of programmable circuits;

a reference generator adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparison circuit adapted to compare the voltage at the first node of the selected programmable circuit to the reference voltage at the second node and to produce an output signal having a binary value indicative of whether the programmable element has been programmed.

37 (previously presented). The apparatus of claim 36, comprising an equilibrating circuitry adapted to equilibrate the voltages at the first and second nodes.

38 (previously presented). The apparatus of claim 36, comprising circuitry adapted to vary the value of the known resistance.

39 (previously presented). The apparatus of claim 36, wherein the comparison circuit comprises a comparator.

40 (previously presented). The apparatus of claim 36, wherein the programmable element comprises an antifuse element.

41 (previously presented). The apparatus of claim 36, wherein the programmable element comprises an ovonic element.

42 (previously presented). An integrated circuit, comprising:

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all programmable circuits being joined in a common connection;

a decoder adapted to decode a first address signal and to send a first enabling signal to each of the plurality of programmable circuits;

a reference circuit adapted to produce a reference voltage at a second node, the reference voltage being based on the value of a known resistance; and

a comparator circuit adapted to compare the voltage at the first node of the selected programmable circuit to the reference voltage at the second node and to produce an output signal having a binary value indicative of whether the programmable element has been programmed.

43 (previously presented). The apparatus of claim 42, wherein the the programmable element comprises an antifuse element.

44 (previously presented). The apparatus of claim 42, wherein the programmable element comprises an ovonic element.

45 (previously presented). A semiconductor memory device, comprising:

a memory array;

a plurality of programmable circuits, each programmable circuit comprising:

a programmable element having a resistance; and

a first node at which a voltage may be developed that is based on the resistance of the programmable element,

wherein the first nodes of all programmable circuits being joined in a common connection;

a circuit adapted to produce a first voltage at a first node based on a known resistance;

a reference circuit adapted to produce a second voltage at a second node based on the resistance of a programmable element; and

a comparison circuit adapted to compare the first voltage to the second voltage and producing an output signal having a binary value in response to the comparison, the binary value of the output signal indicating whether the programmable element has been programmed.

46 (previously presented). The apparatus of claim 45, comprising:

an equilibrating circuit adapted to equilibrate the voltages at the first and second nodes.

47 (previously presented). The apparatus of claim 45, wherein the programmable element comprises an antifuse element.

48 (previously presented). The apparatus of claim 45, wherein the programmable element comprises an ovonic element.